

Preliminary Amendment

Applicant: Andrew Graham et al.

Serial No.: Unknown

(Priority Application No. DE 102 50 868.2)

(International Application No. PCT/DE03/003587)

Filed: Herewith

(Priority Date: October 31, 2002)

(International Filing Date: October 29, 2003)

Docket No.: I432.116.101/P29858

Title: VERTICALLY INTEGRATED COMPONENT, COMPONENT ARRAY AND METHOD FOR FABRICATING (As Amended)

IN THE CLAIMS

Please cancel claims 1-21 without prejudice.

Please add claims 22-43 as follows:

Patent Claims WHAT IS CLAIMED IS:

1-21. (Cancelled)

22. (New) A vertically integrated component comprising:

a first electrically conductive layer;

a middle layer, formed partially from dielectric material, on the first electrically conductive layer;

a second electrically conductive layer on the middle layer; and

a nanostructure integrated in a via hole introduced into the middle layer, the nanostructure further comprising a first end portion that is coupled to the first electrically conductive layer and a second end portion that is coupled to the second electrically conductive layer;

wherein the middle layer, between two adjacent dielectric sublayers, has a third electrically conductive layer, the thickness of which is less than the thickness of at least one of the dielectric sublayers.

23. (New) The component of claim 22, wherein catalyst material for catalyzing the formation of the nanostructure is arranged between the first conductive layer and the nanostructure.

24. (New) The component of claim 23, wherein the third electrically conductive layer surrounds the nanostructure in a region around the first or second end portion.

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25. (New) The component of claim 24, wherein the thickness of the third electrically conductive layer is less than the thickness of both dielectric sublayers.

26. (New) The component of claim 22, further configured as a field-effect transistor, wherein:

the first end portion of the nanostructure forms a first source/drain region and the second end portion of the nanostructure forms a second source/drain region; and

a ring structure formed from an electrically insulating material as gate-insulating region of the field-effect transistor is arranged in the third electrically conductive layer, which forms the gate electrode of the field-effect transistor, along the via hole that has been introduced therein.

27. (New) The component of claim 26, wherein the middle layer has an additional electrically conductive layer, which at least one additional electrically conductive layer serves as an additional gate electrode of the field-effect transistor, with an additional ring structure formed from an electrically insulating material as an additional gate-insulating region of the field-effect transistor being arranged along the via hole that has been introduced in the additional electrically conductive layer.

28. (New) The component of claim 26, having an additional field-effect transistor above the field-effect transistor.

29. (New) The component of claim 28, wherein the field-effect transistor and the additional field-effect transistor are connected to one another as an inverter circuit.

30. (New) The component of claim 22, wherein the first and second electrically conductive layer includes one of a group comprising tantalum, tantalum nitride, titanium,

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molybdenum, aluminum, titanium nitride, and a ferromagnetic material.

31. (New) The component of claims 27, wherein the third and additional electrically conductive layer comprises one of a group comprising polysilicon, tantalum, titanium, niobium, and aluminum.

32. (New) The component of claim 22, wherein the dielectric material of the middle layer is one or a combination of the materials in a group comprising silicon dioxide, silicon nitride, and silicon dioxide doped with potassium ions.

33. (New) The component of claim 22, wherein the nanostructure includes one of a group comprising a nanotube, a bundle of nanotubes, and a nanorod.

34. (New) The component of claim 33, wherein the nanorod includes one of a group comprising silicon, germanium, indium phosphide, gallium nitride, gallium arsenide, zirconium oxide and a metal.

35. (New) The component of claim 33, wherein the nanotube is one of a group comprising a carbon nanotube, a carbon-boron nanotube, a carbon-nitrogen nanotube, a tungsten sulfide nanotube, and a chalcogenide nanotube.

36. (New) The component of claim 23, wherein the nanostructure is a carbon nanotube, and wherein the catalyst material is one of a group comprising iron, cobalt, and nickel.

37. (New) The component of claim 23, wherein the nanostructure is a gallium arsenide nanorod, and wherein the catalyst material includes gold.

38. (New) The component of claim 22, wherein the subregion of the via hole that does

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not have the nanostructure in it is at least partially filled by an electrically insulating spacer structure.

39. (New) The component of claim 22, formed exclusively from dielectric material, metallic material and the material of the nanostructure.

40. (New) The component of claim 22, formed on a substrate made from polycrystalline or amorphous material.

41. (New) A transistor component comprising:
a first conductive layer;
a middle layer on the first conductive layer, the middle layer having a via hole therein;
a second conductive layer on the middle layer;
a nanostructure integrated in the via hole and having a first source/drain region of the transistor that is coupled to the first conductive layer and a second source/drain region of the transistor that is coupled to the second conductive layer; and
means within the middle layer for providing a gate-insulating region of the transistor.

42. (New) The transistor of claim 41, further comprising a third conductive layer in the middle layer between two adjacent dielectric sublayers, wherein the thickness of the third conductive layer is less than the thickness of the dielectric sublayers.

43. (New) A method for fabricating a vertically integrated component, comprising:
forming a first electrically conductive layer;
forming a middle layer partially from dielectric material;
introducing a via hole into the middle layer;
forming a nanostructure having a first end portion and a second end portion in the via hole, the first end portion being coupled to the first electrically conductive layer;

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forming a second electrically conductive layer on the middle layer and coupling the second electrically conductive layer to the second end portion of the nanostructure; and

forming the middle layer in such a manner that a third electrically conductive layer is formed between two adjacent dielectric sublayers, the thickness of which third electrically conductive layer is less than the thickness of at least one of the dielectric sublayers.